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Fast-Transient Radiation-Hardened Low-Dropout Voltage Regulator for Space Applications

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***Abstract*—This paper presents a fast-transient radiation-hardened low-dropout (LDO) voltage regulator integrated in a standard 0.6 μm BiCMOS technology for space and other harsh radiation environments applications. The fabricated LDO consumes 150 μA quiescent current at 6 A maximum output current. A low dropout voltage of 300 mV which corresponds to an ultra-low $R_{DS(ON)}$ resistance of 50 mΩ is realized by accurate modeling. A separate fast-transient response circuit under narrow-bandwidth condition is proposed to improve the output voltage transient speed. It operates from an input voltage range of 2.8 V to 5.5 V and provides an output voltage of 2.5 V, with output voltage accuracy of $\pm 2\%$. The proposed LDO achieves a successful line regulation of 1 mV/V, and a load regulation of 2.16 mV/A. Effective radiation-hardened layout techniques are applied to realise high area-efficient LDO chip, whose total area including pads is 5.35 mm^2, which represents only about one-third area of similar radiation-hardened products. Furthermore, a special set of Total ionising dose (TID) experiments and single event latch-up (SEL) experiments were performed. The measurement results show that the LDO can tolerate up to a total ionising dose (TID) of 150 krad (Si) and SEL immunity at a linear energy transfer (LET) of 99.8 MeV/(mg/cm^2) with proposed layout design.**

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***Index Terms*—Fast-Transient, Low-Dropout (LDO), Single Event Effects (SEE), Total Ionising Dose (TID), Bandgap**

I. Introduction

Energy management and optimization is one of the vital challenges for the battery-powered systems in the space environment such as satellites, launchers and space vehicles operating under harsh conditions with any chance to tolerate any hardware failures. Such systems more frequently face harsh environmental stress such as vibrations, shocks and extreme temperatures in space environment [1]–[3]. On the other hand, in the space environment, flux of high energetic charged particles and gamma rays leads to total ionisation dose (TID) effects in electronic circuits [4], [5], which cause a degradation in performance. Also, the single event effect (SEE) which is the result of a single particle depositing sufficient energy will cause irreparable damage in an electronic device [6]. Hence, the availability of radiation-hardened methodologies offers the possibility of integrated circuits for space applications which include both analog and digital functions of increasing complexity. In this manner, the radiation-hardness of voltage regulator and reference circuits is crucial in the power management unit of space systems [7], [8]. Low-dropout (LDO) regulator provides a constant voltage source, and it is commonly the most essential component in power management modules in space applications [9]–[12].

Table. I shows requirements on total ionising dose (TID) related to different satellite orbits, which is typical requirements for space missions of China. According to standards of in Table. I, for high-earth orbit satellite with a lifetime greater than 12 years, the chip must resist 100 krad (Si) of TID. Moreover, in this high-voltage regulator design, surely that large size transistor with channel length greater than 0.5 μm must be used. Under this circumstance, In general, forward-biased diode, reverse-biased diode, bipolar, power transistor, JFET, MOSFET, and so on can have different resiliency depending on which materials they are made of. For example, bipolar in Silicon is very prone to radiation (the base current increases and the gain degrades, etc.), but bipolar in SiGe overcomes these limitations. Same considerations for MOSFET. If they are fabricated in SOI, they will exhibit better resiliency than those in normal Silicon. Fig. 1 summarises the total dose sensitivity of various common large size semiconductor devices. Generally speaking, for linear IC like LDO, bipolar (especially vertical ones) can resist TID up to 10 krad (Si), but for MOS,

TABLE I
REQUIREMENTS ON TOTAL IONISING DOSE (TID) AND SINGLE EVENT LATCH-UP (SEL) WITH DIFFERENT ORBITS AND LIFETIME

Orbit of Satellite	Lifetime years	Acceptable TID krad (Si)	Unacceptable TID krad (Si)	Acceptable SEL MeV/(mg/cm^2)	Unacceptable SEL MeV/(mg/cm^2)
High-earth orbit	12∼15	100	<50	75	<75
Low-earth orbit	5	30	<10	75	<37

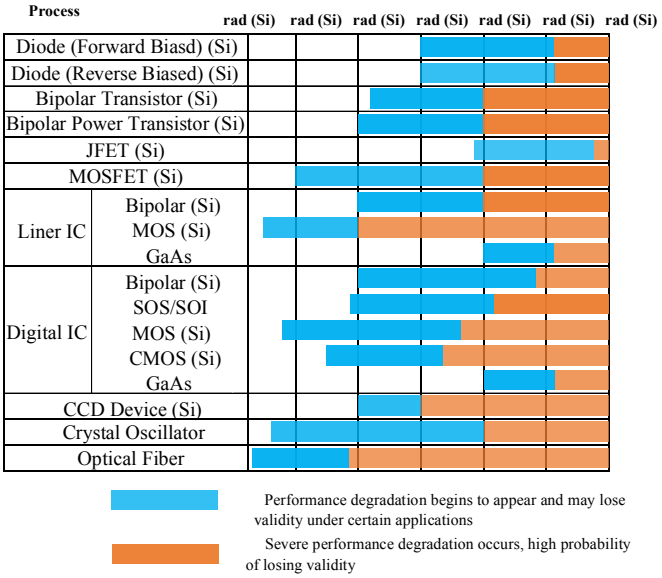

Fig. 1. Diagram of total dose sensitivity of various semiconductor devices.

especially for that one with thick oxides, TID of scarcely 0.5 krad (Si) leads to intense degradation of performance. Therefore, the bipolar device is much more suitable for TID in radiation environment [13], and thus bipolar LDO regulators are of interest for avionics applications because of its much better radiation tolerance resiliency compared to the CMOS technology [14]. Many of them have been in use successfully in space environments for over 10 years. As an alternative to bipolar, the SiGe BiCMOS technology also has application for mixed-signal circuits in emerging extreme environment, since it has stronger TID resilience than the pure BiCMOS at expense of an higher price [15], [16].

On the other hand, as spacecraft designers use increasing numbers of commercial and emerging technology devices to meet stringent performance, testing of such devices for susceptibility to SEE has assumed ever greater importance. The most advanced heavy ion accelerator can provide ^{209} Bi particles for single event latch-up (SEL) experiments. Recent experience in satellite design has also emphasized the innovations on circuit or layout in order to avoid the traditional bulky and costly protective "warm boxes" or "electronics vaults", for example, triple modular redundancy is an effective method to prevent the single event upset [17], furthermore, special layout considerations are needed, in this work, a simple and well-shaped layout is proposed to achieve a high area efficiency.

In this work, the goal is to design a fast-transient radiation-hardened LDO for high-earth orbit satellite applications which target at least 100 krad TID and 75 MeV/(mg/cm^2) linear energy transfer (LET) of SEL immunity. The key contributions of this work can be summarised as follows:

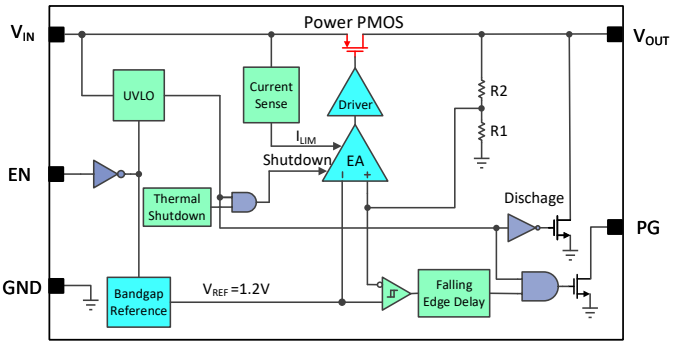

Fig. 2. The functional block diagram of proposed LDO.

1) An area-efficient ultra low dropout voltage of 300 mV has been achieved by implementing several strategies including circuit design, package, etc; The maximum output current reaches the considerable amount of 6 A;
2) An LDO with feed-forward fast-transient response design and class AB driver is proposed to improve the output voltage transient speed under abrupt changes of the output current;
3) It is worth mentioning that the fast-transient radiation-hardened LDO for high-earth orbit satellite applications proposed in this work is a milestone and exhibits a great impact on the aerospace industry of China.

The paper is organised as follows: Section II and Section III describe the circuit design and the main features of the proposed LDO. Section IV shows the layout proposed in this work to improve the radiation tolerance resiliency. Section V introduces the space metal package applied in this work. Section VI discusses the collected experimental results, while the key outcomes are finally summarised in Section VII.

II. SYSTEM OVERVIEW

Fig. 2 shows the functional block diagram of the LDO. The V_{IN} terminal is an input to the regulator, the V_{OUT} terminal provides an output for the load. The LDO chip provides 2.5 V output voltage. The bandgap voltage is typically 1.2 V. The EN terminal is an input which enables or shuts down the device. The comparator makes comparison between the bandgap reference and the fraction of the desired output voltage value, then the PG terminal provides indication for the post-stage circuit. Because the PMOS device behaves as a low-resistance resistor, the dropout voltage is very low (typically 300 mV at an output current of 6A). Additionally, since PMOS power transisotr is a voltage-driven device, the

quiescent current is typically 150 μA at 6 A maximum output current. It is worth mentioning that this LDO is designed to have fast-transient response for large load current changes and also features thermal shutdown protection, under-voltage protection (UVLO) and over-current protection.

III. Circuit Design

Since Fig. 2 is the functional block diagram of proposed LDO, in which the error amplifier and the driver are the most important two sub-blocks. Then, this section introduces the current sense, the error amplifier, the driver and fast transient enhancement design in details.

A. Fast-Transient Response Design

Fig. 3 (a) shows the design proposed featuring fast-transient response, when the output voltage changes dramatically, the drive current immediately changes to improve the slew rate and reduce the LDO undershoot and overshoot. It is based on a classic architecture in which the transient response speed is improved from the following two perspectives: Firstly, the feed-forward path introduced by the Q5 can reduce the loop response time. In the case of dramatic change of output voltage, the change of output directly reflects on emitter of Q5, alters the base voltages of transistors Q6, Q7, Q10 and Q12, then adjusts the input current of the driver so as to adjust the gate voltage of the power transistor $\mathrm{M_P}$, finally, skips the operational amplifier, thereby reduces the loop delay, and improves the transient response speed; Secondly, class-AB driver is used to improve the transient response speed.

B. Loop Stability Considerations

The LDO has been designed for high stability and low drop out operation. The device requires a minimum of 1 μF input capacitor and requires the use of output capacitor for frequency compensation. It requires a minimum of 100 μF output capacitor $\mathrm{C_L}$ to ensure stability, but $\mathrm{C_L}$ is suggested to be small to improve the response time. Thus, there is a contradiction between the stability and the transient-response improvement. There are many ways to speed up the transient response of LDO. An approach proposed in [18] uses a 600-pF on-chip capacitor to reduce the output voltage ripple, unfortunately, this bulky capacitor does not meet the power saving and area-limited requirements of SOC designs. In [19], an active-frequency compensation scheme is applied to extend the loop bandwidth drastically, and the required on-chip capacitance is reduced to 0.4 pF. In [11], an inverter-based dynamic loop is added to alter the bias current of amplifier according to the load in order to improve the transient response, but has increased the circuit complexity. With regard to the above concerns, in this work, fast-transient response is designed independently under the condition of narrow loop bandwidth, the proposed transient enhancement scheme can greatly boost the transient response and only require small additional circuit on a typical LDO configuration.

As shown in Fig. 3 (a), the main loop consists mainly of an operational amplifier, transient enhancement circuit (which includes a feed-forward path and a discharge path), a class-AB driver and an output power transistor. The amplifier is a second-stage amplifier with Miller compensation. The class-AB driver improves the bidirectional slew rate of the output power transistor. The equivalent small signal model of Fig. 3 (a) is shown in Fig. 3 (b), where g_{m1} and g_{m2} is the first-stage and the second-stage transconductance of the amplifier, respectively, g_{m3} is the equivalent transconductance of the class-AB driver, and G_{mp} is the transconductance of the power transistor, r_{oeq} is the parallel resistance of the power transistor and the load. When the feedback loop is open, the transfer function T(S) of the loop is derived as in Eq. 1, here, $A_{openloop}$ is the open-loop gain of the amplifier, obviously, $A_{openloop} = g_{m1} \cdot r_{o1} \cdot g_{m2} \cdot r_{o2} \cdot G_{mp} \cdot r_{oeq}$, F is the feedback factor, referred as $\frac{R_{f2}}{R_{f1}+R_{f2}}$. In total, three poles and two zeros exist in the whole system (Eq. 2 $\sim$ Eq. 6): amplifier with Miller compensation provides one low-frequency main pole (Eq. 2), one high-frequency pole (Eq. 4) and one zero (Eq. 6), another pole is contributed by the output capacitor and output equivalent resistance (Eq. 3), the other ESR zero is caused by the output capacitor and its series resistance (Eq. 5).

$$P_{-3\mathrm{dB}} = \frac{1}{2\pi \cdot r_{o1} \cdot g_{m2} \cdot r_{o2} \cdot C_c} \tag{2}$$

$$P_{1nd} = \frac{1}{2\pi \cdot r_{oeq} \cdot C_L} \tag{3}$$

$$P_{2nd} = \frac{1}{2\pi \cdot r_{o2} \cdot C_c} \tag{4}$$

$$Z_1 = \frac{1}{2\pi \cdot R_{ESR} \cdot C_L} \tag{5}$$

$$Z_2 = \frac{1}{2\pi \cdot R_c \cdot C_c} \tag{6}$$

$$\begin{aligned} PM = 180^0 &+ \arctan\frac{\omega_u}{Z_1} + \arctan\frac{\omega_u}{Z_2} \\ &- \arctan\frac{\omega_u}{P_{-3dB}} - \arctan\frac{\omega_u}{P_{1nd}} - \arctan\frac{\omega_u}{P_{2nd}} \end{aligned} \tag{7}$$

In order to ensure loop stability with different load, Miller compensation capacitor is applied to push the high-frequency pole as far as possible, so that there is only one pole in the whole loop. Assuming that only one pole is within the loop unity gain frequency, it needs to be satisfied $10P_{-3\mathrm{dB}} < \omega_u < \frac{P_{1nd}}{10}$ and $P_{1nd} < P_{2nd}$, then $PM \approx 90^\circ$ (Eq. 7). For $\omega_u = A_{openloop} \cdot F \cdot P_{-3\mathrm{dB}} = \frac{F \cdot g_{m1} \cdot G_{mp} \cdot r_{oeq}}{2\pi \cdot C_c}$, it must satisfy $\frac{r_{oeq} \cdot C_L}{r_{o2}} > C_c > 10F \cdot g_{m1} \cdot G_{mp} \cdot r_{oeq}^2 \cdot C_L$, F $= \frac{R_{f2}}{R_{f1}+R_{f2}}$. In this case, the pole and zero distribution of the system loop is shown in Fig. 3 (c).

The simulation results of loop gain and phase are shown in Fig. 4, which validate the aforementioned analysis and derivations. The bandwidth and phase margin of loop is 2.3 kHz and 56 degrees without load respectively; In case of full load, the bandwidth and phase margin of loop is 2.5 kHz and 87 degrees. In this work, system bandwidth is sacrificed for system stability, resulting in excessive phase margin.

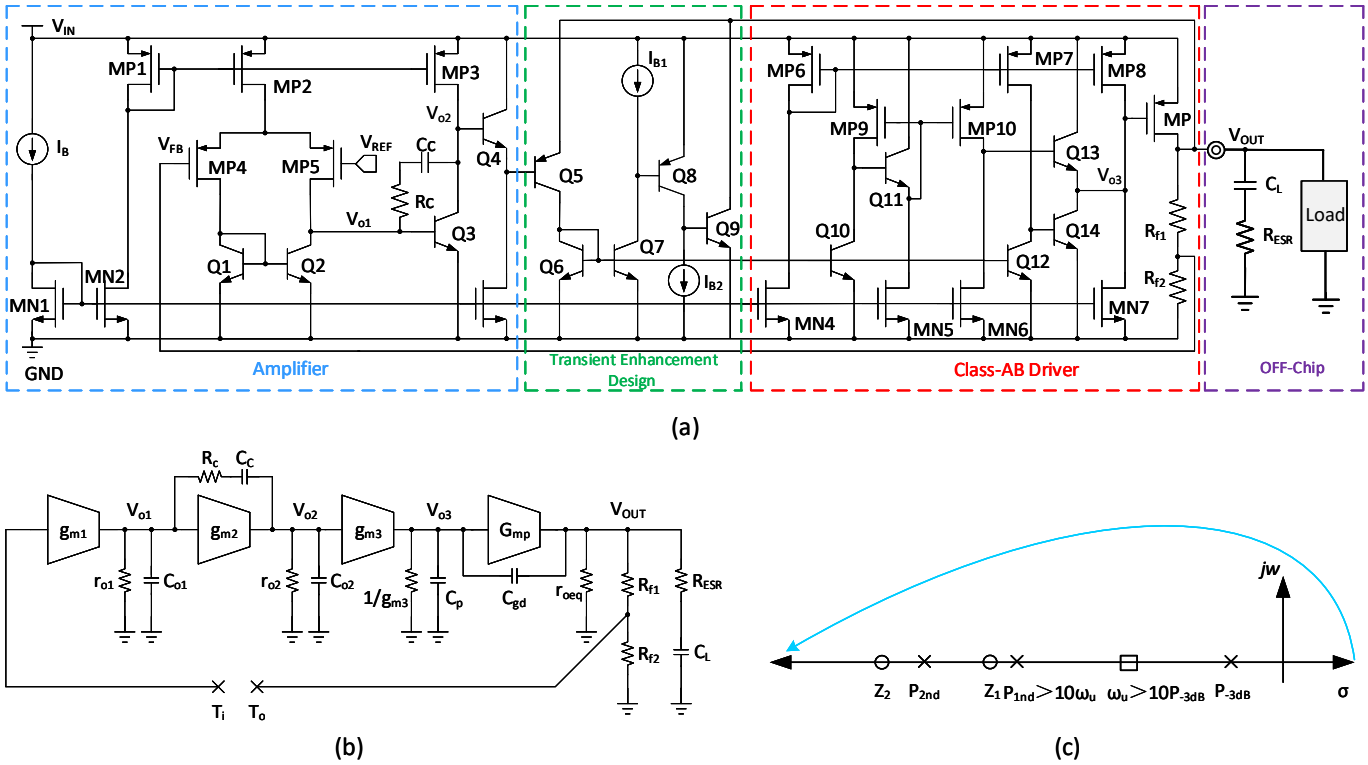

Fig. 3. (a) Block diagram of the proposed LDO with fast-transient response; (b) equivalent small signal circuit model; and (c) pole and zero distribution of the system loop.

$$T(S)=\frac{T_o(S)}{T_i(S)}\approx -\frac{g_{m1}\cdot r_{o1}\cdot g_{m2}\cdot r_{o2}\cdot G_{mp}\cdot r_{oeq}\frac{R_{f2}}{R_{f1}+R_{f2}}(1+S\cdot R_c\cdot C_c)(1+S\cdot R_{ESR}\cdot C_L)[1-S\frac{(1-g_{m2}\cdot R_c)C_c}{g_{m2}}](1-S\frac{C_{gd}}{G_{mp}})}{(1+S\cdot r_{o1}\cdot g_{m2}\cdot r_{o2}\cdot C_c)(1+\frac{R_c\cdot C_{o1}}{g_{m2}\cdot r_{o2}})(1+S\cdot r_{o2}\cdot C_c)(1+S\cdot R_c\cdot C_{o2})(1+\frac{C_p+C_{gd}\cdot G_{mp}\cdot r_{oeq}}{g_{m3}})(1+S\cdot r_{oeq}\cdot C_L)(1+S\cdot R_{ESR}\cdot C_{gd})}$$
$$\approx -\frac{g_{m1}\cdot r_{o1}\cdot g_{m2}\cdot r_{o2}\cdot G_{mp}\cdot r_{oeq}\frac{R_{f2}}{R_{f1}+R_{f2}}(1+S\cdot R_{ESR}\cdot C_L)(1+S\cdot R_c\cdot C_c)}{(1+S\cdot r_{o1}\cdot g_{m2}\cdot r_{o2}\cdot C_c)(1+S\cdot r_{oeq}\cdot C_L)(1+S\cdot r_{o2}\cdot C_c)}\approx -\frac{A_{openloop}\cdot F(1+\frac{S}{Z_1})(1+\frac{S}{Z_2})}{(1+\frac{S}{P_{-3dB}})(1+\frac{S}{P_{1nd}})(1+\frac{S}{P_{2nd}})} \quad (1)$$

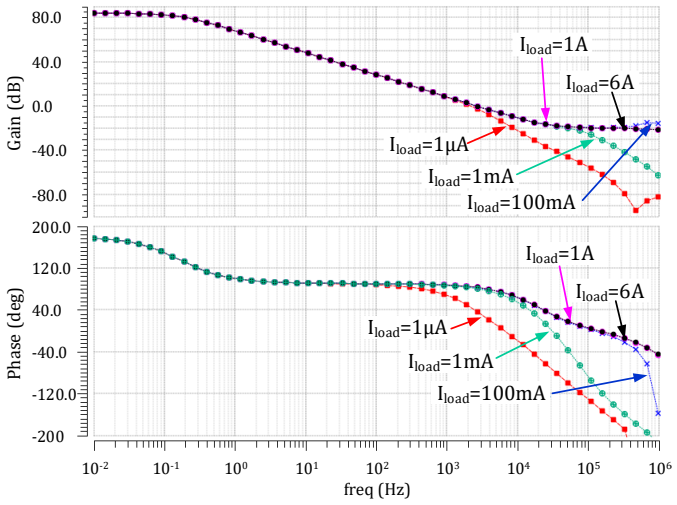

Fig. 4. Simulation result of loop gain.

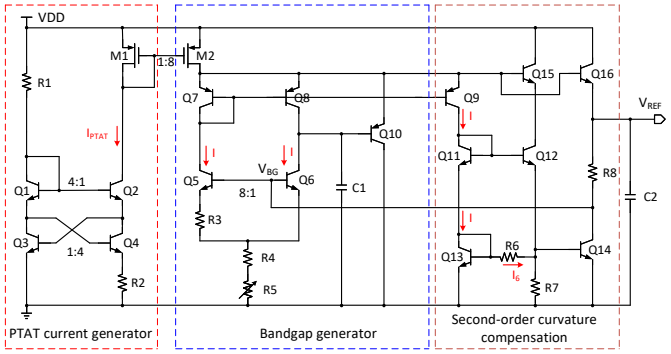

Fig. 5. The whole circuit of the bandgap reference.

C. Bandgap Voltage Reference Circuit

A precise bandgap voltage reference is an essential component in a variety of analog and mixed signal electronic devices. The bandgap core in this work gets rid of the need of an amplifier, then the complexity of the circuit is decreased as well. Considering now the circuit of Fig. 5, the proposed second-order compensated bandgap reference consists of a PTAT current generator, a bandgap circuit and a second-order curvature compensation circuit.

The PTAT current generator consists of Q1, Q2, Q3, Q4 and R2, here, $I_{C1}=I_{C3}$, $I_{C2}=I_{C4}$, $I_{S1}=4I_{S3}$ and $I_{S4}=4I_{S2}$,

ignore base currents, then leads

$$I_{PTAT} = \frac{\Delta V_{BE2,4} + \Delta V_{BE3,1}}{R_2} = \frac{KT}{qR_2}\ln(16) \quad (8)$$

In Eq. (8), $\Delta V_{BE2,4} = V_{BE2} - V_{BE4}$ and $\Delta V_{BE3,1} = V_{BE3} - V_{BE1}$.

The bandgap generator consists of Q5, Q6, Q7, Q8, Q10, Q16 and R3, R4, R5, where R5 is an adjustable resistor for trimming, here, the ratio of Q5 to Q6 is 8:1, then bandgap voltage V_{BE6} is generated as follows:

$$\begin{aligned} V_{BG} &= V_{BE6} + 2\frac{\Delta V_{BE_{6,5}}}{R_3}(R_4 + R_5) \\ &= V_{BE6} + 2\frac{KT}{q}\ln(8)\frac{(R_4 + R_5)}{R_3} \end{aligned} \quad (9)$$

The second-order curvature compensation circuit is composed of Q11, Q12, Q13, Q14 and R6, R7, R8. The collector current of Q14 (I_{14}) which goes through R8 is a second-order compensation component, superimposed on the reference voltage V_{BG} to finally form a compensated reference voltage V_{REF}. During the derivation, all base currents are ignored:

$$I_6 R_6 = V_{BE_{12,11}} = V_T ln\frac{\frac{V_{BE14}}{R_7} - I_6}{I_S} - V_T ln\frac{I}{Is} \quad (10)$$

$$I = I_6 + I_s e^{\frac{V_{BE14} + I_6 R_6}{V_T}} \approx I_s e^{\frac{V_{BE14} + I_6 R_6}{V_T}} \quad (11)$$

Due to Eq. (11), it can be derived:

$$I_6 \approx \frac{V_T \ln(\frac{I}{I_s}) - V_{BE14}}{R_6} = \frac{V_{BE11} - V_{BE14}}{R_6} \quad (12)$$

Substituting the Eq. (12) into the Eq. (10):

$$V_T \ln(\frac{I}{I_s}) - V_{BE14} + V_T \ln(\frac{I}{I_s}) = V_T \ln \frac{\frac{V_{BE14}}{R_7} + \frac{V_{BE14} - V_{BE11}}{R_6}}{I_s} \quad (13)$$

Organize the above Eq. (13):

$$\frac{V_{BE14}}{V_T} = \ln\left(\frac{(\frac{I}{I_s})^2 I_s}{\frac{V_{BE14}}{R_7} + \frac{V_{BE14} - V_{BE11}}{R_6}}\right) \quad (14)$$

Then,

$$I_{14} = I_s e^{\frac{V_{BE14}}{V_T}} = \frac{(\frac{\Delta V_{BE_{6,5}}}{R_3})^2}{\frac{V_{BE14}}{R_7} + \frac{V_{BE14} - V_{BE11}}{R_6}} \quad (15)$$

Therefore, the final bandgap reference voltage is :

$$\begin{aligned} V_{REF} &= V_{BE6} + 2V_T \ln(8)\frac{(R_4 + R_5)}{R_3} + I_{14}R_8 \\ &\approx V_{BE6} + 2V_T \ln(8)\frac{(R_4 + R_5)}{R_3} + \\ &\frac{R_8}{{R_3}^2}(\ln(8))^2 \frac{{V_T}^2}{\frac{V_{BE14}}{R_7} + \frac{\Delta V_{BE_{14,11}}}{R_6}} \end{aligned} \quad (16)$$

In (16), the second-order temperature compensation is generated. Finally, conventional poly fuse trimming is applied on resistor R5 in order to calibrate the drift of the bandgap reference caused by the mismatch. The minimum step for trimming is 1 mV, the optimum temperature coefficient is achieved by 6 separate trimming points including 1 mV, 2 mV, 4 mV, 8 mV, 16 mV and 32 mV.

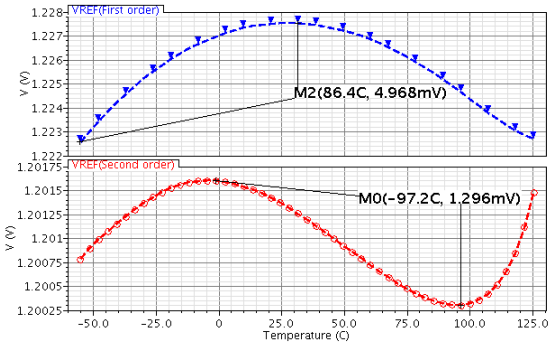

Fig. 6. Simulated Bandgap output voltage with first-order (top) and second-order (bottom) compensation.

Fig. 6 shows the nominal simulation of the bandgap output voltage, for a temperature swept from $-55°$C to 125°C. Before the second-order curvature compensation, the typical value of bandgap is 1.225 V, the variance of bandgap voltage with temperature is 4.968 mV, corresponding to the percent change in bandgap voltage of 0.4%, therefore, the temperature coefficient (TC) is 22.5 ppm/°C; After the curvature compensation, the typical value of bandgap is 1.201 V, the variance of bandgap voltage with temperature is only 1.296 mV (0.1% change in bandgap voltage), therefore, the TC has been dropped to 6 ppm/°C with the curvature compensation.

IV. Layout

The effects of radiation on transistors can easily compromise the correct behaviour of analog blocks. Therefore, special layout considerations are needed. As concerns the TID tolerance, at first, Fig. 7 (a) and Fig. 7 (b) show the conventional ring-gate layout designs used to mitigate the effect [20], [21], in that case, routing will become much more complicated, and it is difficult to calculate the W/L ratio of MOS device accurately. Furthermore, it is clear that the use of n-channel MOSFETs always leads a significant increase in subthreshold leakage current with increasing total-dose irradiation. Therefore, adjusting the substrate voltage should increase the threshold voltage V_{th} to improve the radiation hardness [22]. Fig. 7 (c) shows the improved NMOS ring-gate layout applied in this work. In Fig. 7 (c), ring-gate surrounds the drain region, and since the field oxide region is only adjacent to the N+ active region, internal leakage will not occur. Moreover, adjacent NMOS transistors with guard rings will provide further isolation without parasitic MOS. However, due to a large number of MOS transistors, ring-gate layout cannot be applied to every device to prevent the total dose effects. Therefore, other than ring-gate layout (Fig. 7 (c)) proposed is applied, conventional annular-gate and H-gate (not shown here) are all used in the actual layout design.

For the PMOS power transistor, comb-shaped gate sometimes has been applied to improve the TID tolerance, as shown in Fig. 8 (a). This design shows good performance in terms of TID tolerance, but there are a large number of sharp corner,

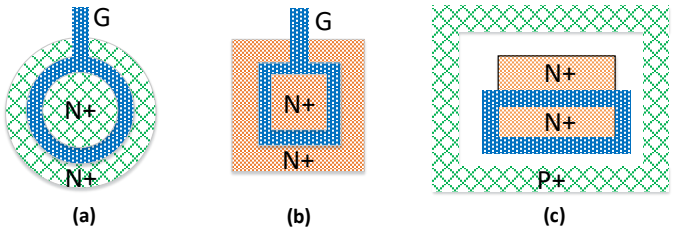

Fig. 7. (a) Conventional NMOS ring-gate layout (circle); (b) Conventional NMOS ring-gate layout (square); (c) Proposed NMOS ring-gate layout.

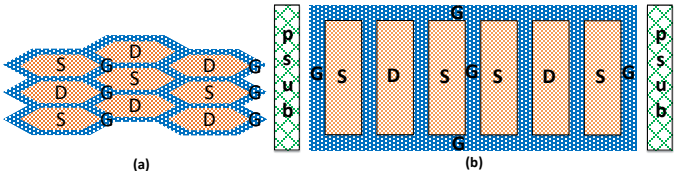

Fig. 8. (a) Traditional comb-shaped gate for the PMOS power transistor; (b) Proposed layout for the PMOS power transistor in this work.

and the resiliency for single event effect and ESD is not satisfactory.

In order to prevent potential MOS parasitics appearing in the field due to the total dose, after many trial and error process, we found out the proposed layout design for PMOS power transistor shown in Fig. 8 (b) as the best solution. Compared with the comb-shaped gate, the proposed layout for PMOS power transistor can decrease the routing complexity greatly.

It is worth mentioning that the layout proposed is much more area-efficient than the similar product in [23], the total area including pads in this work is only 5.35 mm^2 (1.37mm $\times$ 3.91mm), while the total area of similar radiation-hardened product in [23] is 17.82 mm^2, also, measured TID and SEL tolerance in this work shows significant benefits with respect to [23].

V. Space Hermetic Metal Packages

In the dropout region, the power transistor acts like a resistor with a value equal to the drain-to-source on resistance, $R_{DS(ON)}$. Typically, $R_{DS(ON)}$ includes resistance from the power transistor, on-chip interconnects, bondwires and package leads. So, in this work, the package is carefully designed to realise a 300 mV ultra-low dropout voltage with a 6 A load current even when packaged.

In general, hermetically sealed metal package is applied for space and military applications. There are two methods for the interconnection between the chip and the substrate, that is, conductive adhesive and eutectic welding. Compared with conductive adhesive, the eutectic welding is especially much more suitable for the welding of extreme environmental requirements.

Since the Au80Sn20 alloy solder has excellent properties such as high strength, high thermal conductivity and fluxfree at soldering, it has been widely used in space qualified device [24]. The use of a molybdenum (Mo) substrate allows high-temperature operation.

Internally, the conductor material used for package electrical routing is tungsten (W), and the bondwires are made of Au. To decrease the resistance of wire, bondwires are in parallel connection, 9 1-mm gold wires constitute R_{BOND1} (left of Fig. 9 (a)), and 6 1.5-mm gold wires constitute R_{BOND2} (right of Fig. 9 (a)), where L, D and m refer to lead length, bondwire diameter, and number of bondwires in parallel connection respectively, R_{Au1}, R_{Au2} refer to resistance of a single bondwire.

Fig. 9 (b) shows the equivalent resistance contribution in the ceramic package, $R_{SILICON}$ is the on-resistance of the LDO, R_{BOND1} is the bondwire equivalent resistance between the chip and the ceramic substrate, R_{SUB} corresponds to the resistance of ceramic substrate, R_{BOND2} is the equivalent resistance between the ceramic substrate and leadframe, and R_{LEAD} is the resistance of the lead. Finally, the total resistance from input to output equal to 46.58 mΩ, accordingly, Table. II summarises the packing materials and equivalent resistance.

TABLE II
Description of Packaging Materials and Equivalent Resistance

Resistance name	Details	Equivalent Resistance
$R_{SILICON}$	PMOS on resistance	21mΩ
R_{BOND1}	Au (Diameter=50μm)	1.44mΩ
R_{SUB}	Wu is plated with Au (1.5μm) and Ni (2μm)	5mΩ
R_{BOND2}	Au (Diameter=50μm)	3.25mΩ
R_{LEAD}	Copper core is plated with Au (1μm) and Ni (4μm)	3.1mΩ

VI. Experiment Results

The proposed LDO regulator was fabricated using the 0.6-μm BiCMOS technology. Fig. 10 shows the chip photo. The whole area of prototype is 1.37mm $\times$ 3.91mm including pads (core area is 0.944mm $\times$ 3.54mm=3.34 mm^2). The size of the power transistor is 400000μm/0.6μm to provide high output current. The dropout voltage is 300 mV.

The chip has fast-transient response for large load current changes. Fig. 11 shows the undershoot and the overshoot output voltages of the proposed LDO regulator are 45 and 45 mV respectively, with its settling time of 50 μs.

The performance of the proposed LDO keeps constant over the whole temperature range.

As shown in Fig. 12(a), the variance of quiescent current is about 56 μA over the whole temperature range from -55°C to 125°C and in Fig. 12(b), the variance of V_{OUT} is smaller than 0.12% over the whole temperature range. It is worth mentioning that quiescent current and output voltage shifts in Fig. 12 were measured before radiation, because the irradiation environment does not provide low and high temperatures test.

Fig. 13 (a) illustrates the measured load regulation performance of the proposed architecture for load current variation from 1 mA load current to 6 A load current. The variance of V_{OUT} is 13 mV, and the LDO achieves 2.16 mV/A load

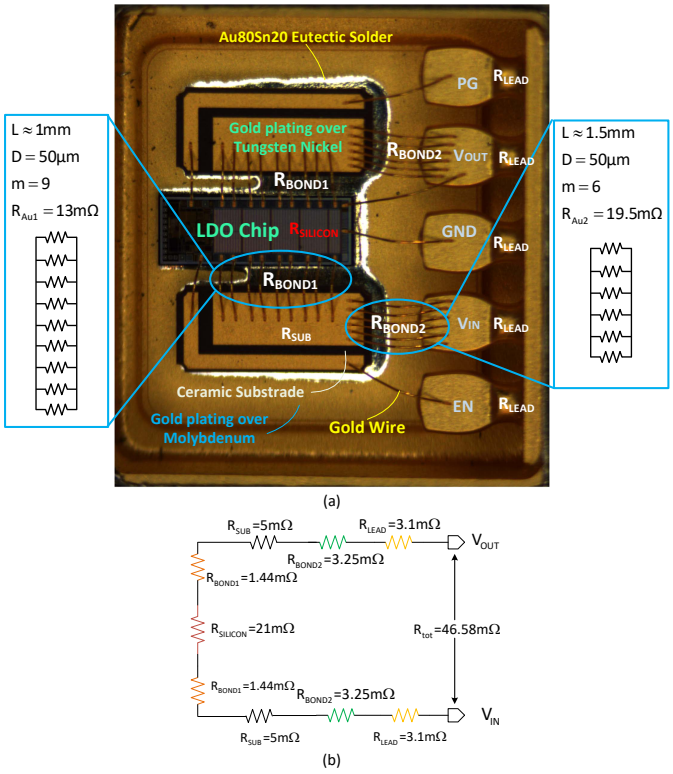

Fig. 9. (a) Metal package of the proposed LDO chip; (b) Total resistance contribution of the metal package.

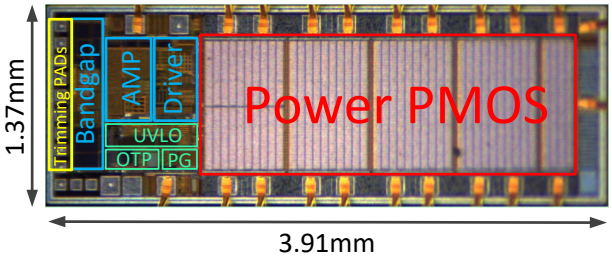

Fig. 10. The fabricated LDO microphotograph: whole chip including pads.

regulation. The line regulation results of the LDO is depicted in Fig. 13 (b). With a load current I_{OUT} of 1 mA, V_{IN} changes from 3.5 V to 5.5 V, the variance of V_{OUT} is 2 mV, the proposed LDO achieves less than 1 mV/V line regulation.

The irradiations were performed using a Cobalt-60 gamma ray source. Fig. 14 and Fig. 15 reflect drain current and V_{th}

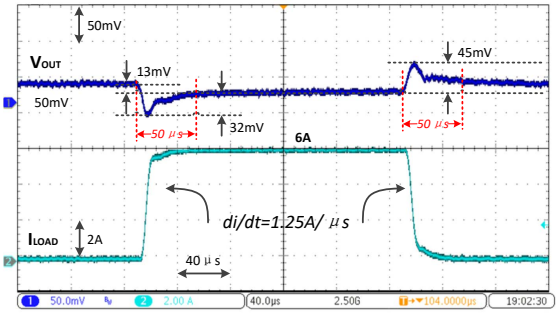

Fig. 11. Measured transient response for 6 A load current.

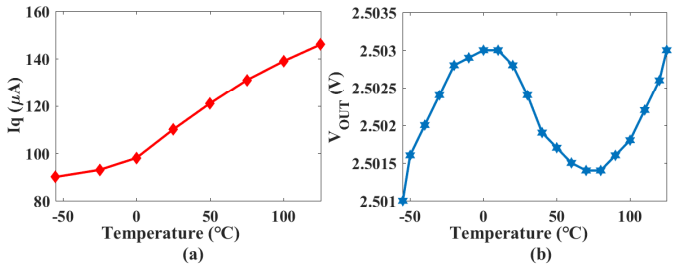

Fig. 12. (a) Quiescent Current (b) Output Voltage shifts versus Temperature.

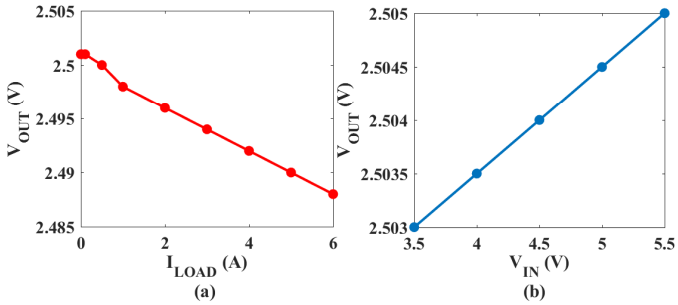

Fig. 13. (a) Measured load regulation; (b) Measured line regulation.

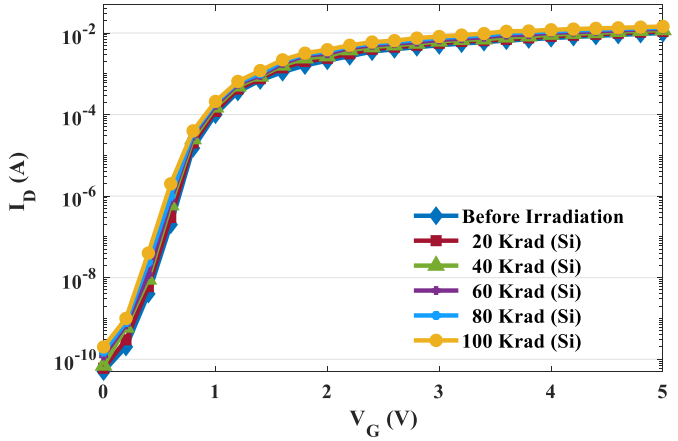

Fig. 14. Drain current of test NMOS sample with the total ionizing dose.

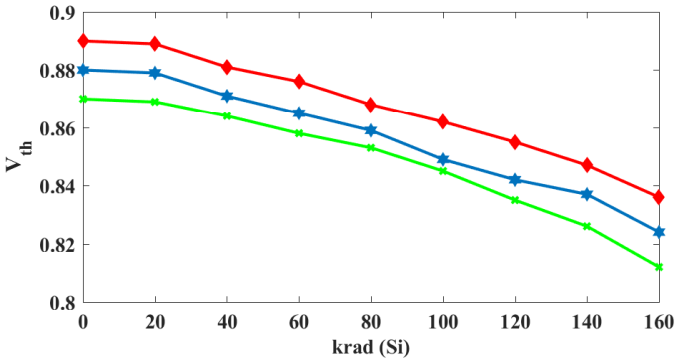

Fig. 15. V_{th} variance of three test NMOS samples with the total ionizing dose.

variance of NMOS with the total ionising dose respectively. Test NMOS sample has shown that the drain current almost

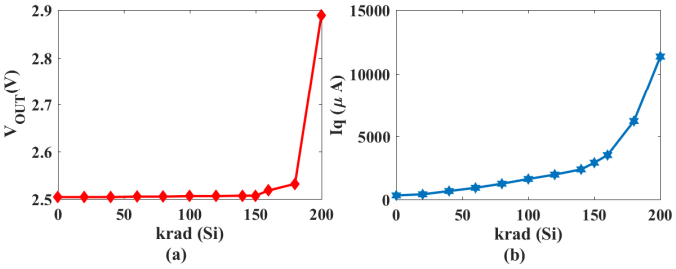

Fig. 16. Measured output voltage V_{OUT} (a) and quiescent current I_q (b) versus radiation exposure.

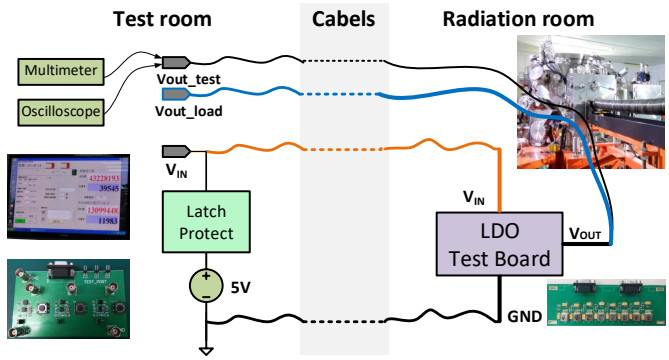

Fig. 17. Measurement Setup of Heavy Ion Research Facility.

remained stable at the total-dose of about 80 krad (Si) and V_{th} did not have obvious fluctuation at the total-dose of about 150 krad (Si), which demonstrates that the layout applied in this work is effective enough to resist total dose effect.

In TID experiments, the chip was irradiated by a ^{60}Co source at room temperature at dose rate of 6 rad (Si)/s under bias. Fig. 16 reflects the resilience to total-dose effects. In Fig. 16 (a), the output voltage V_{OUT} measured at an input voltage of 5 V increases monotonically with dose for exposure up to 150 krad (Si), till 200 krad (Si), the change in V_{OUT} increases dramatically as it is not be able to provide a stable output voltage of 2.5 V. Also, in Fig. 16 (b), the quiescent current I_q increases dramatically for exposure up to 150 krad (Si). Results of Fig. 16 demonstrate that the LDO is qualified to 150 krad(Si) and can satisfy demands for high-earth orbit satellite applications.

Heavy ion tests were completed by using the advanced heavy ion accelerator. The set-up is shown in Fig. 17, it can provide five kinds of particles (proton, ^{12}C, ^{86}Kr, ^{112}Sn, and ^{209}Bi) for all series experiments. The experiment data for radiation-hardened chip were obtained using ^{209}Bi ions and the maximum LET of ^{209}Bi applied in the experiment is able to achieve at the value of 99.8 MeV/(mg/cm^2). All tests were conducted in the air under the normal incidence. Fig. 18 shows measured output voltage V_{OUT} and I_{VDD} versus radiation exposure at an LET of 99.8 MeV/(mg/cm^2), it can be seen that sudden transients do not occur for the output voltage V_{OUT} and the current of power supply I_{VDD}. The maximum variance of V_{OUT} is only 0.4%.

Some similar commercial products and academic research works are compared with the proposed LDO, as shown in

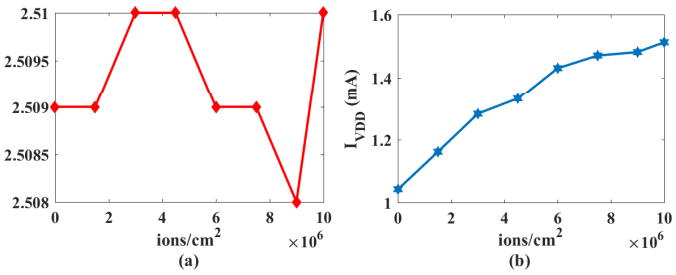

Fig. 18. Measured output voltage V_{OUT} (a) and power supply current I_{VDD} (b) versus radiation exposure at an LET of 99.8 MeV/(mg/cm^2).

Table III. Among all the products, the proposed LDO can provide the maximum 6 A output current and can tolerate up to single event latch-up immunity at a linear energy transfer (LET) of 99.8 MeV/(mg/cm^2). Compared with similar product exploiting radiation-hardened design, this work has much better area efficiency. The total area including pads in this work is 5.35 mm^2, only about one-third area of similar radiation-hardened products of [23], whose area is 17.82 mm^2, also, measured TID and SEL tolerance in this work show significant benefits with respect to [23], which demonstrate the advantages of adopting radiation-hardened layout design. Academic research work [25] can achieve low dropout voltage and good load regulation, but 29.7 mV of low dropout voltage in [25] is realized by NMOS power transistor, which needs dual power supplies, then increases the system complexity, and [25] does not provide the data of V_{OUT} when I_{OUT} is smaller than 30 mA. Also, [25] does not consider the wide temperature operation and radiation hardness design. [26] has achieved a maximum 3A output current with excellent line and load regulation, but the quiescent current reaches 3 mA. [27] and [28] have better total ionising dose because their pure bipolar technology, but the dropout voltage and quiescent current are much larger, also, the line regulation of [27] is worse than the proposed product. Although [29] has achieved the similar line and load regulation, but no radiation hardness design is considered in [29].

VII. Summary

This LDO proposed is intended for space and harsh radiation environments. Novel layout-level radiation-hardened techniques are employed to improve the radiation tolerant abilities. The radiation experiments show that the circuit survived a 150 krad(Si) total ionizing dose without degradation in function, and the LDO achieves SEL immunity at a linear energy transfer (LET) of 99.8 MeV/(mg/cm^2).

VIII. Acknowledgments

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TABLE III
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART

	This work	[29]	[23]	[27]	[28]	[26]	[25]
Supply Voltage (V)	$2.8 \sim 5.5$	$2.8 \sim 5.5$	$1.5 \sim 7$	$3 \sim 12$	$2.9 \sim 6.5$	$2.2 \sim 5.5$	$1.05 \sim 2.0$
Maximum Output Current (A)	6	5	3	3	3	3	0.3
Technology	BiCMOS	BiCMOS	BiCMOS	Bipolar	Bipolar	BiCMOS	CMOS
Operating temperature (°C)	$-55 \sim 125$	$-40 \sim 125$	$-55 \sim 125$	$-55 \sim 125$	$-55 \sim 125$	$-55 \sim 125$	27
Output voltage accuracy (%)	± 2	± 2	± 2	± 2	± 5	0.5	-
Quiescent Current (μA)	150	125	7000	100000	-	3000	120
Dropout Voltage (mV)	300 (I_{out}= 6A)	250 (I_{out}= 5A)	210 (I_{out}= 3A)	950 (I_{out}= 2A)	1100 (I_{out}= 3A)	200 (I_{out}= 3A)	29.7 (I_{out}= 0.3A)
Load Transient Response ΔV_{out} (mV)	45 (ΔI_{out}= 6A)	120 (ΔI_{out}= 5A)	27 (ΔI_{out}= 0.3A)	-	-	51 (ΔI_{out}= 3A)	56 (ΔI_{out}= 0.3A)
Load Reg. (mV)	13	21.8	25	12.5	-	1.6	1.8
Line Reg. (mV)	2	2	3	8.75	-	0.3	0.396
Single Event Latch-up ($MeV/mg/cm^2$)	99.8	-	85	FREE	84	-	-
Total Ionizing Dose (krad (Si))	150	-	100	300	1000	-	-

REFERENCES

[1] S. Bonaldo and S. Mattiazzo and C. Enz and A. Baschirotto and D. M. Fleetwood and A. Paccagnella and S. Gerardin, "Ionizing-Radiation Response and Low-Frequency Noise of 28-nm MOSFETs at Ultrahigh Doses," *IEEE Transactions on Nuclear Science*, vol. 67, no. 7, pp. 1302–1311, 2020.

[2] C. Calligaro and U. Gatti, *Rad-hard Semiconductor Memories*. River Publisher, 2018.

[3] G. Ciarpi and S. Saponara, "Inductorless DC/DC Converter for Aerospace Applications With Insulation Features," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 9, pp. 1659–1663, 2020.

[4] T. Vergine, M. De Matteis, S. Michelis, G. Traversi, F. De Canio, and A. Baschirotto, "A 65 nm Rad-Hard Bandgap Voltage Reference for LHC Environment," *IEEE Transactions on Nuclear Science*, vol. 63, no. 3, pp. 1762–1767, 2016.

[5] T. F. Miyahira and B. G. Rax and A. H. Johnston, "Total dose degradation of low-dropout voltage regulators," in *IEEE Radiation Effects Data Workshop.*, 2005, pp. 127–131.

[6] R. Sorge, J. Schmidt, C. Wipf, F. Reimer, R. Pliquett, and T. Mausolf, "JICG MOS transistors for reduction of radiation effects in CMOS electronics," in *2018 IEEE Topical Workshop on Internet of Space (TWIOS)*, 2018, pp. 17–19.

[7] A. Privat and P. W. Davis and H. J. Barnaby and P. C. Adell, "Total Dose Effects on Negative and Positive Low-Dropout Linear Regulators," *IEEE Transactions on Nuclear Science*, vol. 67, no. 7, pp. 1332–1338, 2020.

[8] M. V. O'Bryan, K. A. LaBel *et al.*, "Radiation damage and single event effect results for candidate spacecraft electronics," in *Radiation Effects Data Workshop*, 2000, pp. 106–122.

[9] R. L. Pease and G. W. Dunham and J. E. Seiler, "Total Dose and Dose Rate Response of Low Dropout Voltage Regulators," in *IEEE Radiation Effects Data Workshop*, 2006, pp. 85–93.

[10] J.-H. Lin, Y.-S. Ma, C.-M. Huang, L.-C. Lin, C.-H. Cheng, K.-H. Chen, Y.-H. Lin, S.-R. Lin, and T.-Y. Tsai, "A high-efficiency and fast-transient digital-low-dropout regulator with the burst mode corresponding to the power-saving modes of DC-DC switching converters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2018, pp. 314–316.

[11] Y. Huang, Y. Lu, F. Maloberti, and R. P. Martins, "Nano-Ampere Low-Dropout Regulator Designs for IoT Devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 4017–4026, 2018.

[12] Y. Lu, F. Yang, F. Chen, and P. K. Mok, "A 500mA analog-assisted digital-LDO-based on-chip distributed power delivery grid with cooperative regulation and IR-drop reduction in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2018, pp. 310–312.

[13] A. Hassan, Y. Savaria, and M. Sawan, "Electronics and Packaging Intended for Emerging Harsh Environment Applications: A Review," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2085–2098, 2018.

[14] T. H. Kim and H. C. Lee, "Total Ionizing Dose Effects on a 12-bit 40kS/s SAR ADC Designed With a Dummy Gate-Assisted n-MOSFET," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 648–653, 2017.

[15] L. Najafizadeh, A. K. Sutton, R. M. Diestelhorst, M. Bellini, B. Jun, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "A comparison of the effects of X-Ray and proton irradiation on the performance of SiGe precision voltage references," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2238–2244, 2007.

[16] L. Najafizadeh, M. Bellini, A. G. Prakash, G. A. Espinel, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "Proton tolerance of SiGe precision voltage references for extreme temperature range electronics," *IEEE Transactions on nuclear science*, vol. 53, no. 6, pp. 3210–3216, 2006.

[17] H. Fan, D. Li, K. Zhang, Y. Cen, Q. Feng, F. Qiao, and H. Heidari, "A 4-Channel 12-Bit High-Voltage Radiation-Hardened Digital-to-Analog Converter for Low Orbit Satellite Applications," *IEEE Trans. Circuits Systems I: Regular Papers*, vol. 65, no. 11, pp. 3698–3706, 2018.

[18] P. Hazucha, T. Karnik, B. A. Bloechel *et al.*, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, 2005.

[19] H.-C. Lin, H.-H. Wu, and T.-Y. Chang, "An active-frequency compensation scheme for CMOS low-dropout regulators with transient-response improvement," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 9, pp. 853–857, 2008.

[20] N. Chen, T. Wei, X. Wei, and X. Chen, "A radiation hardened sram in 180-nm rhbd technology," in *2013 IEEE 11th International Conference on Dependable, Autonomic and Secure Computing*, 2013, pp. 159–162.

[21] J. Verbeeck, P. Leroux, and M. Steyaert, "Radiation effects upon the mismatch of identically laid out transistor pairs," in *IEEE Int. Conf. Microelectronic Test Structures (ICMTS)*, 2011, pp. 194–197.

[22] J. Riffaud and M. Gaillardin and C. Marcandella and N. Richard and O. Duhamel and M. Martinez and M. Raine and P. Paillet and T. Lagutere and F. Andrieu and S. Barraud and M. Vinet and O. Faynot, "TID Response of Nanowire Field-Effect Transistors: Impact of the Back-Gate Bias," *IEEE Transactions on Nuclear Science*, vol. 67, no. 10, pp. 2172–2178, 2020.

[23] Texas Instruments, "Ultra-Low Dropout (LDO) Regulator," *TPS7H1101 Datasheet*, [Online]. Available: www.ti.com.

[24] C. Yang, L. Li, and Y. Xue, "Study on preparation process of Au80Sn20 eutectic solder on thin film substrate," in *Int. Conf. Electronic Packaging Technology (ICEPT)*, 2018, pp. 450–453.

[25] Q.-H. Duong, H.-H. Nguyen, J.-W. Kong, H.-S. Shin, Y.-S. Ko, H.-Y. Yu, Y.-H. Lee, C.-H. Bea, and H.-J. Park, "Multiple-loop design technique

for high-performance low-dropout regulator," *IEEE Journal of Solid-state Circuits*, vol. 52, no. 10, pp. 2533–2549, 2017.

[26] H. Fan and X. Diao and Y. Li and K. Fang and H. Wen and D. Li and K. Zhang and Y. Cen and D. Zhang and Q. Feng and H. Heidari, "An External Capacitor-Less Low-Dropout Voltage Regulator Using a Transconductance Amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1748–1752, 2019.

[27] STMicroelectronics, "RAD-HARD POSITIVE FIXED VOLTAGE REGULATORS," *RHFL4913 Datasheet*, [Online]. Available: www.st.com.

[28] International Rectifier, "Ultra Low Dropout Positive Fixed Linear Regulator ," *IRUH33P183A1M Datasheet*, [Online]. Available: www.irf.com.

[29] Texas Instruments, "FAST-TRANSIENT RESPONSE 5-A LOW-DROPOUT VOLTAGE REGULATORS," *TPS75525 Datasheet*, [Online]. Available: www.ti.com.